IN THE SPECIFICATION:

Please amend the paragraph on page 23 beginning at line 23 as follows:

--Fig. 10 schematically shows a cross sectional structure taken along the line L10-L10 shown in Fig. 9. Referring to Fig. 10, memory cells are formed on a P type (silicon) substrate 69 [[70]]. NMOS region 40, PMOS region 41 and NMOS region 42 are delimited by P well, N well and P well, respectively, and thus, the MOS regions and the corresponding well regions are denoted by the same reference characters. N wells 66 and 67 for forming P channel MOS transistors of adjacent memory cells are formed on the outsides of P wells 40 and 42, respectively.--

Please amend the paragraph on page 27 beginning at line 14 as follows:

--Fig. 14 shows a configuration of a main portion of the PMOS substrate control circuit. Referring to Fig. 14, N well 41 is formed on a P type substrate 69 [[74]]. P channel MOS transistors to be arranged in one column are formed in N well 41. N wells 80 and 81 are formed on a surface of P type substrate 69 [[70]], isolated from N well 41 by element isolation regions 85b and 85c. N wells 80 and 81 are further isolated from other cell formation regions by element isolation regions 85a and 85d. A P channel MOS transistor (pass transistor) P1 for transmitting a high voltage Va is formed in N well 80. A P channel MOS transistor (pass transistor) P2 for transmitting a low voltage Vb is formed in N well 81.—

AMENDMENTS TO THE DRAWINGS:

The attached sheets of drawings includes changes to Figures 10 and 14.

The first sheet, which includes Figures 9 and 10, replaces the original sheet including Figures 9 and 10. In Figure 10, the reference number "70" has been changed to "69".

The second sheet, which includes Figures 13 and 14, replaces the original sheet including Figures 13 and 14. In Figure 14, the reference number "70" has been changed to "69".

Attachments: Replacement Sheet
Annotated Sheet Showing Changes